Sensor Interface Circuit

EDM710 Product Description

EDC

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1.0 GENERAL

This specification describes an Application Specific Integrated Circuit (EDM710) which was designed to condition and digitize the differential signal from a piezoresistive bridge accelerometer. TheEDM710 shall have two synchronous serial ports; one for analog circuit configuration data and one for digitized signal output data. The EDM710 is intended to be used with a microcontroller (µC) to allow closed loop control of gain and offset to counteract the effects of temperature on the accelerometer. A temperature sensor internal to the chip allows determination of current temperature. A buffered clock output and open drain power on reset are also included to facilitate low parts count operation with a µC. A block diagram of the EDM710 is included in figure 1.

2.0 GENERAL ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximums

Voltage: 7.0V
Configuration serial clock: 1.0 MHz
Data serial clock: 1.0 MHz
Master clock: 16 MHz

2.2 Operating Conditions

Voltage: 4.5 V to 5.0 V
Current: 1.5 mA typ, 5 mA max

2.3 Temperature

Storage: -60°C to 100°C
Operating: -40°C to 85°C

2.4 Military Requirements:

The die shall be 100% electrically tested at ambient temperature to the performance requirements of this specification. A sample from each lot shall be electrically tested at the minimum and maximum operating temperatures specified in 2.3 to the performance requirements of this specification. The die shall be 100% visually inspected in accordance with MIL-STD-883D method 2010 level B.

3.0 I/O ELECTRICAL CHARACTERISTICS

3.1 Analog Inputs

The following characteristics apply to the INN, INP, and ADIN pins. The INN pin is the negative input, and INP is the positive input to the instrumentation amplifier. The ADIN pin is an external input to the multiplexer which controls the input to the analog to digital converter.

R_{in}: 1 MΩ minimum
I_{in}: 1 mA maximum
C_{in}: 50 pF maximum
Noise RFI: TBD nV/√Hz maximum

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3.2 Analog Output

3.2.1 Switched Capacitor Filter (SCF)

The SCF output is a direct analog output from the SCF.

V_{PP}, Minimum output swing: V_{REF} ± 1.5 V
I_{OUT}, Minimum output current: 50 mA
R_L, Minimum output load to V_{REF}: 30 kΩ
R_S, output impedance: 2.0 kΩmaximum

3.3 Digital Inputs

The Test pin controls the functioning of the multiplexer (mux) and the SCF output in a manner to facilitate testing of the ASIC. The test pin has an internal 10 mA pull down transistor to reduce bonding requirements. The CS pin is the chip select which enables the transfer of data to and from the mC. The CDL pin enables the latch for the configuration data input from the mC. The CDI pin is the input for the configuration data from the mC. The CDC pin is the clock input from the mC which controls the transfer of data from the mC to the ASIC. The SDC pin is the clock input which controls the transfer of sensor data from the ASIC to the mC. The CDC and CDL pins are disabled when CS is low.

Pins: Test, CS, CDL, CDI, CDC, SDC
R_{in}, minimum input resistance: 1 MΩ
I_{in}, maximum leakage current: 1 mA
C_{in}, maximum input capacitance: 10 pF
V_{INH}, minimum input voltage for guaranteed HI: 0.8 V_{DD}
V_{INL}, maximum input voltage for guaranteed LOW: 0.2 V_{DD}
I_{PD}, minimum pull down current on TEST pin: 10 mA

3.4 Digital Output

The CDO pin allows the mC to verify the previous configuration data sent to the ASIC. The D9/PD3/SDO pin is used to transfer sensor data from the ASIC to the mC when in the serial or parallel data transfer modes. The D8/PD2, D7/PD1, D6/PD0 pins are used to transfer data in the 10 bit and 4 bit parallel modes. The D5, D4, D3, D2, D1, D0 pins are used only in the 10 bit parallel mode. The CLKOUT pin is a buffered master clock output for use by the mC, its frequency is the same as the oscillator configured on OSCIN and OSCOUT. CDO and D0 through D9 are high impedance when CS is low.

Pins: CDO, D9/PD3/SDO, D8/PD2, D7/PD1, D6/PD0, D5, D4, D3, D2, D1, D0, CLKOUT
I_{HI}, max output current for guaranteed HI: 200 mA
I_{IL}, max input current for guaranteed LOW: 200 mA
V_{OH}, min voltage at max output current for HI: 0.8 VDD
V_{OL}, max voltage at max input current for LOW: 0.2 VDD

3.5 Special Function Pins

3.5.1 VREF

The V_{REF} pin is a buffered output tied to the on chip analog ground.
I_{REF}, min output current for V_{REF}: ± 150 mA
V_{REF}, output voltage for I_{REF}: V_{DD}/2 ± 50 mV

3.5.2 BIAS

The BIAS pin allows the user to increase or decrease the current drive and consequently the gain bandwidth of the opamps in the ASIC.

R_{BIAS}, Resistance to V_{DD}: 100 kΩ internal
Resistance to V_{SS}: TBD minimum

3.5.3 Power On Reset (POR)

The POR pin is a power on reset, implemented as an open drain transistor with a 30 kΩ pullup resistor. The transistor pulls down the POR line when the power supply voltage is between 1.5 V and 4.0 V.

I_{OL}, maximum sink current for V_{OL}: 200 mA
V_{OL}, maximum voltage for I_{OL}: 0.2 V_{DD}
I_{LH}, maximum leakage current for HI: 5 mA

3.5.4 OSCIN and OSCOUT

The OSCIN and OSCOUT pins are used for generating the master clock on the ASIC. It has been implemented as a linear oscillator to minimize current consumption. The oscillator will support both crystals and ceramic resonators.

Min frequency: 1 MHz
Max frequency: 16 MHz

4.0 FUNCTION BLOCKS

4.1 Sensor Channel

The sensor channel is designed for resistive bridge sensors. The input is an instrumentation amplifier (INAMP). The reference voltage for the INAMP is adjustable through the digital configuration data. The anti-alias filtering for the ADC is accomplished with a four pole continuous time low pass filter, and a 4-pole Butterworth low pass switched capacitor filter. Adjustable gain is built into the antialiasing filters. The analog components are all digitally controlled by a Configuration Data Word 32 bits long which is described in detail in section X.

4.1.1 Instrumentation Input Amp (INAMP)

The INAMP is a standard 3 opamp design utilizing low noise opamps for the inputs, and having a adjustable gain of 3dB or 23 dB. The Gain is selected by the CDW, bit DI31, with DI31 high selecting 23dB and DI31 low selecting 3dB.

Maximum input signal (@ 23dB): ± 75mV
Maximum input signal (@ 3dB): ± 750mV
Gain (DI31 Hi): 23 dB ± 1 dB
Gain (DI31 Lo): 3 dB ± 1 dB
Min input common mode range: 1V -4V (10mV input signal)
Max input offset voltage: TBD

4.1.2 Reference Adjustment Circuit

The reference adjustment circuit is used to compensate for DC offset of the sensor and is composed of two subcircuits, the coarse adjustment, and the fine adjustment. The coarse adjustment should be set for individual sensors and thereafter left alone. The fine adjustment circuit should be used to cancel temperature dependent offset changes. The total offset correction equals the coarse adjustment plus the fine adjustment.

Total adjustment range: V_{REF} - 480 mV to V_{REF} + 607 mV
Maximum settling time: 1.5 ms

4.1.3 Coarse Offset Adjustment Circuit

The coarse offset adjustment circuit is a 4 bit DAC ranging from AGND ± 480 mV. The control bits are DI20 through DI23 of the configuration data word (CDW). It is controlled by binary increments as shown in the following table. See Section 5 for information on the CDW.

Adjustment range: V_{REF} ± 480 mV (-34mV/+43mV)
Step size: 64 mV ± 2%

Coarse Offset Control

DI23	DI22	DI21	DI20	Coarse Adj. V_{REF} + X mV
0	0	0	0	-480
0	0	0	1	-416
-	-	-	-	-
0	1	1	1	-32
1	0	0	0	+32
-	-	-	-	-
1	1	1	0	+496
1	1	1	1	+480

4.1.4 Fine Offset Adjustment Circuit

The fine offset adjustment circuit is a 7-bit DAC ranging from 0 to 127 mV. The control bits are DI8 through DI14 of the CDW. It is controlled by binary increments as shown in the following table.

Adjustment range: 0 to 127 mV ±2%
Step Size: 1 mV ± 2%
Monotonicity: ± 1 LSB

Fine Offset Control

DI14	DI13	DI12	DI11	DI10	DI9	DI8	Fine Adj. mV
0	0	0	0	0	0	0	+0
0	0	0	0	0	0	1	+1
-	-	-	-	-	-	-	-
1	0	0	0	0	0	0	+64
-	-	-	-	-	-	-	-
1	1	1	1	1	1	1	+127

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4.1.5 Anti-Alias Filters

The anti-alias filter is composed of two low pass sections. The first section is a 4-pole continuous time filter which prevents aliasing in the switched capacitor filter. This filter also contains the coarse gain adjustment. The second section is a 4-pole Butterworth switched capacitor filter. This filter has an adjustable cut off frequency as well as the fine gain adjustment.

Total Gain = 3 dB + InAmp Gain + Coarse Gain + Fine Gain

4.1.5.1 Continuous Filter

The continuous filter is a pseudo Butterworth low pass filter with 4 poles and a selectable corner frequency of 500 Hz or 2 kHz. The corner frequency is selected by control bit DI7 of the CDW. The coarse gain control is also implemented in this section and is controlled by control bits DI16 through DI19 of the CDW. The coarse gain can be adjusted from 0 dB to 45 dB in 3 dB steps by binary increments of DI16 through DI19 as shown in the following table.

Coarse Gain Range: 0 to 45 dB
Coarse Gain Step Size: 3 dB
Gain Accuracy: Gain setting ±5%

DI7	Frequency Response (f_c)
0	0.5 to 1.0 kHz
1	2kHz to 4 kHz

Coarse Gain Control

DI19	DI18	DI17	DI16	Gain (dB)
0	0	0	0	0
0	0	0	1	3
0	0	1	0	6
0	1	0	0	12
1	0	0	0	24
1	1	1	1	45

Note: Coarse Gains over 36 dB not recommended for use.

4.1.5.2 Switched Capacitor Filter

The SCF is a Butterworth low pass filter with 4 poles whose cutoff frequency is adjustable by varying the SCF clock frequency. The SCF clock frequency is generated by dividing the master clock. The divider ratio is controlled by control bits DI28 through DI30 of the CDW as shown in the first table. The corner frequency of the filter is the SCF clock divided by 256. The fine gain has also been implemented in this circuit and is controlled by control bits DI0 through DI6 of the CDW. The fine gain ranges from 3 to 8.967 dB in steps of 0.047 dB, and is controlled by binary increments of DI0 through DI6 as shown in the second table.

Corner Frequency Control

DI30	DI29	DI28	Master/SCF Clock Ratio	Corner Freq. Master Clock = 4 MHz (Hz)
0	0	0	1024	15.3
0	0	1	512	30.5
0	1	0	256	61.0
0	1	1	128	122.1
1	0	0	64	244.1
1	0	1	32	488.3
1	1	0	16	976.6
1	1	1	8	1953.1

SCF clock to f_{3dB}: 256:1
Max SCF clock freq.: 512 kHz
3 dB frequency accuracy: ±1% typical, ±2% max

Fine Gain Control

DI6	DI5	DI4	DI3	DI2	DI1	DI0	Gain (dB)
0	0	0	0	0	0	0	3
0	0	0	0	0	0	1	3.047
0	0	0	0	0	1	0	3.094
0	0	0	0	1	0	0	3.188
0	0	0	1	0	0	0	3.375
0	0	1	0	0	0	0	3.75
0	1	0	0	0	0	0	4.50
1	0	0	0	0	0	0	6.00
1	1	1	1	1	1	1	8.953

Fine gain range: 3.000 to 8.953 dB
Fine gain step size: 0.047 dB
Accuracy: ±5%
Monotonicity: ±1 LSB

4.1.6 Multiplexer (MUX)

The mux is a 4 channel multiplexer whose output goes to the Analog to Digital Converter (ADC). The mux is controlled by control bits DI24 and DI25 of the CDW. When the temperature sensor is selected, the mux will change when the new configuration data word is latched. After the temperature sensor sample is taken the mux will revert back to the analog channel.

Mux Control

DI25	DI24	Selection TEST LO	Selection TEST HI
0	0	Analog Channel	Analog Channel
0	1	External Input	Offset DAC
1	0	SCF Bypass	SCF Bypass
1	1	Temperature Sensor	Temperature Sensor

4.1.7 Analog To Digital Converter (ADC)

The ADC is a 10 bit SAR converter implemented with switched capacitors. The sampling rate is controlled by DI26 and DI27 of the CDW, and can be selected from 2 to 16 times the SCF corner frequency.

Range: 3 V
Resolution: 10 bits
Step Size: 2.93 mV
Monotonicity: ±1 LSB, ±0.5 LSB typical
Conversion time: 16 x SCF clock period

Output code of Analog to Digital Converter

Voltage @ Input	Output Code (MSB D 90, D80, D70, D60, D50, D40, D30, D20, D10, D00 LSB)
V_{REF} + 1.4985 V	1111111111
V_{REF} + 1.4956 V	1111111110
-	-
V_{REF} + 1.46 mV	10000000000
V_{REF} - 1.46 mV	01111111111
_	-
V_{REF} - 1.4956 V	0000000001
V_{REF} - 1.4985 V	0000000000

Sampling Rate Control

DI27	DI26	Sampling Ratio Sample Rate/ SCF F_{3dB}	Sample Clock for SCF (Hz) f_{3dB}=244.1 Hz
0	0	2:1	488.3
0	1	4:1	976.6
1	0	8:1	1953.1
1	1	16:1	3906.2

Sampling time: SCF clock period
Maximum clock frequency: 512 kHz
Minimum conversion time: 31.2 ms
Maximum sampling rate: 32 kHz

5.0 TEST MODES

The ASIC shall have a TEST pin to reconfigure the ADIN pin and SCF pin. When the test pin is high, pin ADIN will be connected to the offset adjustment DAC, and SCF will be connected to the ADC multiplexer output. The automatic rollover for the temperature setting of the ADC mux shall be disabled in test mode.

6.0 SERIAL INTERFACE

Define: Input as data from µC to EDM710
Output as data from EDM710 to µC

6.1 Configuration Data Word Input

The input port is activated when CS is high. The data is clocked into the ASIC using the CDC pin. The CDI pin is the input to a 32 bit shift register as the new 32 bits of configuration data word are clocked in, the previous configuration data word will be shifted out the CDO pin. The data is read on the rising edge of CDC and the design is static so the clock may be irregular. Maximum CDC clock rate is 1 MHz. The MSB of block A (DI31) is sent first. When all 32 bits have been clocked into the configuration data word input, a rising edge on the CDL pin enables the data latch. The data is latched on the following Conversion Complete (CNVC) signal from the ADC. See figure 2 for a timing diagram.

If the CDW configures the multiplexer for a temperature sensor sample, the sample will be available on the CNVC pulse after the CNVC pulse which latches the CDW. The multiplexer will automatically revert back to sampling the sensor channel after the temperature sensor sample is taken. One sensor channel data point will be replaced with a temperature data point.

6.1.1 Input Pin Configuration

5 line interface, 3 lines minimum (CDI, CDC, CDL).

1. Chip Select (CS)
2. Configuration Data In (CDI)
3. Configuration Data Out (CDO)
4. Configuration Data Clock (CDC)
5. Configuration Data Latch (CDL)

6.1.2 Configuration Data Word (CDW) Description

The CDW data shall be 4 bytes long, with the following format:

	MSB			LSB
CDW bit #	31	23	15	7
DATA BLOCK	ABBBCCDD	EEEEFFFF	GHHHHHHH	IJJJJJJ
	Byte 1	Byte 2	Byte 3	Byte 4

The definition of the data blocks are as follows:

A	INAMP GAIN	1 bit	In Amp gain setting
B	SCF CLOCK	3 bits	Master clock (CLKOUT) divide setting
C	SAMPLE CLOCK	2 bits	Sample clock divide setting
D	MULTIPLEXER	2 bits	Select input to ADC
E	COARSE OFFSET	4 bits	Coarse offset setting
F	COARSE GAIN	4 bits	Coarse gain setting
G	PAR/SER	1 bit	Selects parallel(0) or serial(1) port
H	FINE OFFSET	7 bits	Offset adjustment setting
I	FILTER SELECT	1 bit	Selects 5 kHz(0) or 20 kHz(1) continuous filter
J	FINE GAIN	7 bits	Fine gain setting

6.1.3 CDW Power On Configuration

The power on configuration, with resulting data for CLKOUT = 4 MHz in parentheses, is as follows:

A	1	In Amp gain = 23 dB
B	100	SCF clock = CLKOUT / 64 (62.5 kHz), SCF f_c = SCF clk / 256 (244 Hz)
C	10	ADC sample rate = 8 x SCF f_c (1.95 kHz)
D	00	Sensor channel, (11 is temperature sensor)
E	0111	AGND - 32mV
F	0000	Minimum gain + 0dB
G	1	Serial mode
H	0100000	Coarse offset setting + 32mV (Sensor Reference = AGND)
I	0	500 Hz continuous filter
J	1000000	Minimum gain + coarse gain + 3dB (Total 29 dB)

6.2 Analog to Digital Converter Data Output

The output port is activated by chip select CS high, when CS is low the outputs are high impedance. All 10 bits of data are valid 100 nsec after the rising edge of CNVC. In addition the data can be clocked out in a serial or 4 bit parallel mode. See figure 3 for a timing diagram. Conversion Complete (CNVC) is a positive logic output pulse indicating when a new ADC result is available for transfer. The duration of the pulse is CLKOUT/4, which is 1 ms for a 4 MHz clock on CLKOUT. The conversion time for the ADC is 16 cycles of the SCF clock.

6.2.1 Output Pin Configuration

13 lines for interface, 3 lines minimum in serial mode (SDC, SDO, CNVC).

1. Chip Select (CS) - same as for input
2. Sampled Data Out Clock (SDC)
3. Data Out 9 (D9O/PD3/SDO)
4. Data Out 8 (D8O/PD2)
5. Data Out 7 (D7O/PD1)
6. Data Out 6 (D6O/PD0)
7. Data Out 5 (D5O)
8. Data Out 4 (D4O)
9. Data Out 3 (D3O)
10. Data Out 2 (D2O)
11. Data Out 1 (D1O)
12. Data Out 0 (D0O)
13. Conversion Complete (CNVC)

6.2.3 Serial Output Data Description

In serial mode, the data shall be shifted out SDO with the MSB first. The MSB of the ADC result will be valid 100 nsec after the rising edge of CNVC. The subsequent data will be valid 100 nsec after the rising edge of SDC.

	MSB									
A/D result	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SDC Clock #	0	1	2	3	4	5	6	7	8	9
SDO	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

6.2.3 Parallel Output Data Description

In parallel mode, the data shall be clocked out PD4, PD3, PD2 and PD1. The ADC results D9, D8, D7 and D6 will be valid 100 nsec after the rising edge of CNVC. The subsequent data will be valid 100 nsec after the rising edge of SDC.

SDC Clock #	**0**	**1**	**2**
PD3	D9	D5	D1
PD2	D8	D4	D0
PD1	D7	D3	0
PD0	D6	D2	0

7.0 TEMPERATURE SENSOR

The sensor is a ratiometric temperature sensor using matched bipolar transistors and exploiting the variation in the base to emitter voltage over temperature.

Temperature sensing range: -40°C to 70°C
Typical resolution: 9.0 mV/C (0.3 C/ADC bit)
Designed voltage output:

Temp (C)	Voltage
-40	V_{REF} - 474mV
+70	V_{REF} + 473mV

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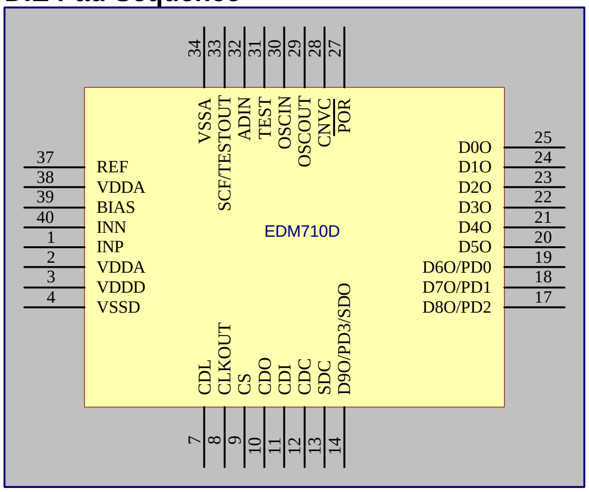
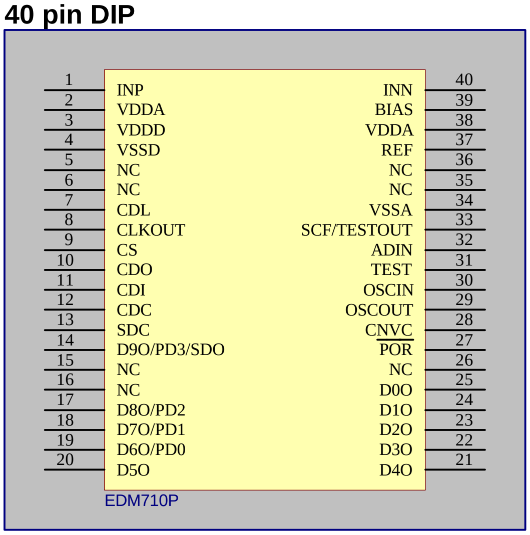
8.0 MECHANICAL DIMENSION

The die size shall be 133 mils by 112 mils, and shall have the pads arranged as shown below. The EDM710 will have the following package options and pinouts: 40 pin DIP denoted by suffix P, and a 32 pin PLCC denoted by the suffix L.

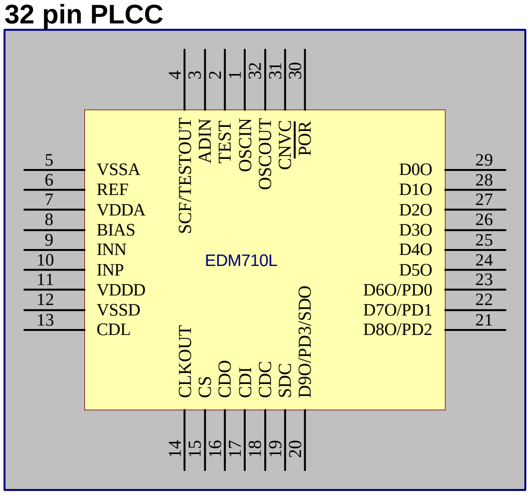
DIE Pad Sequence



40 pin DIP



32 pin PLCC



EDM710 Block Diagram

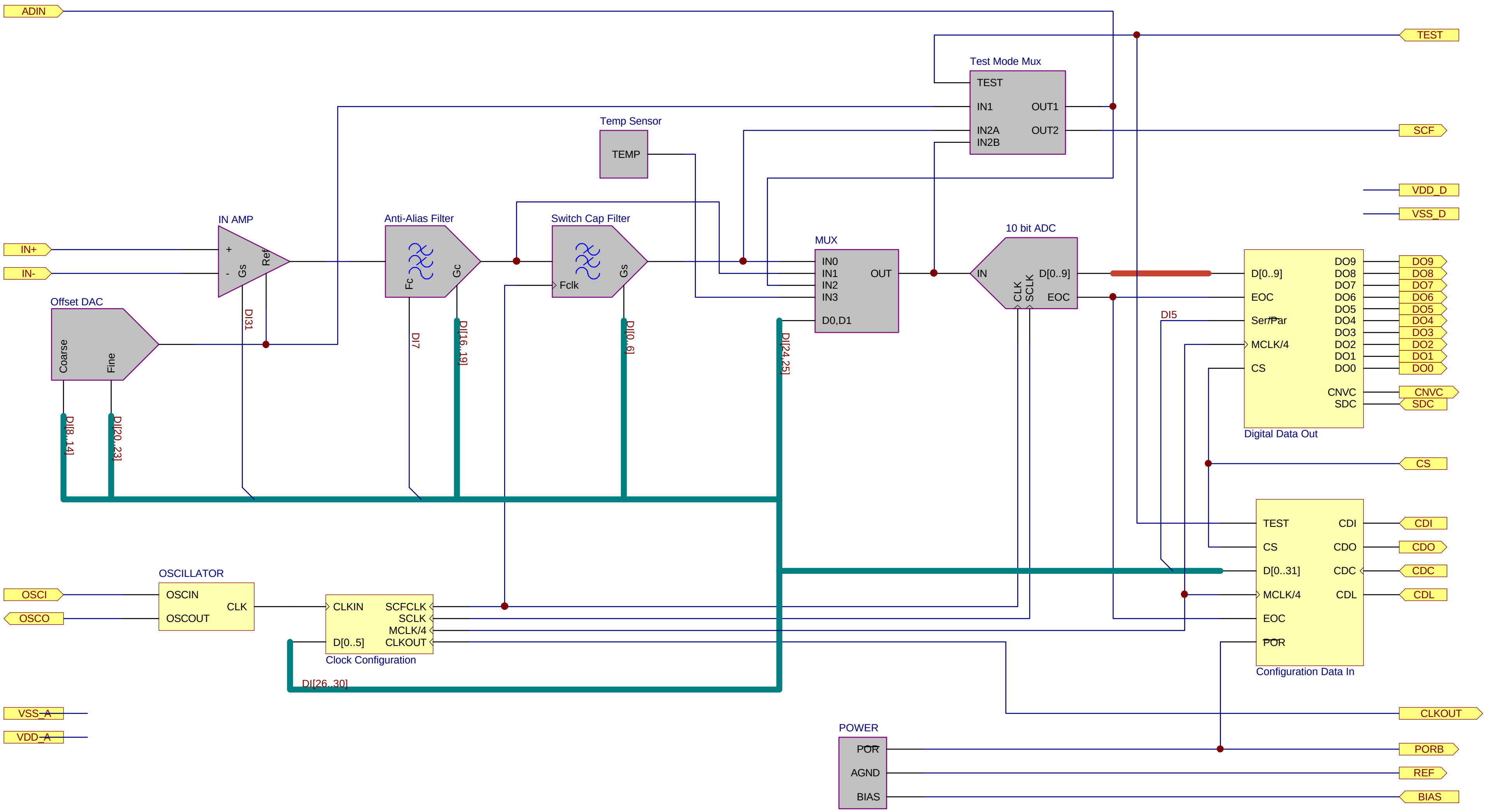


Figure 1

Timing Diagram for Configuration Data Word Input

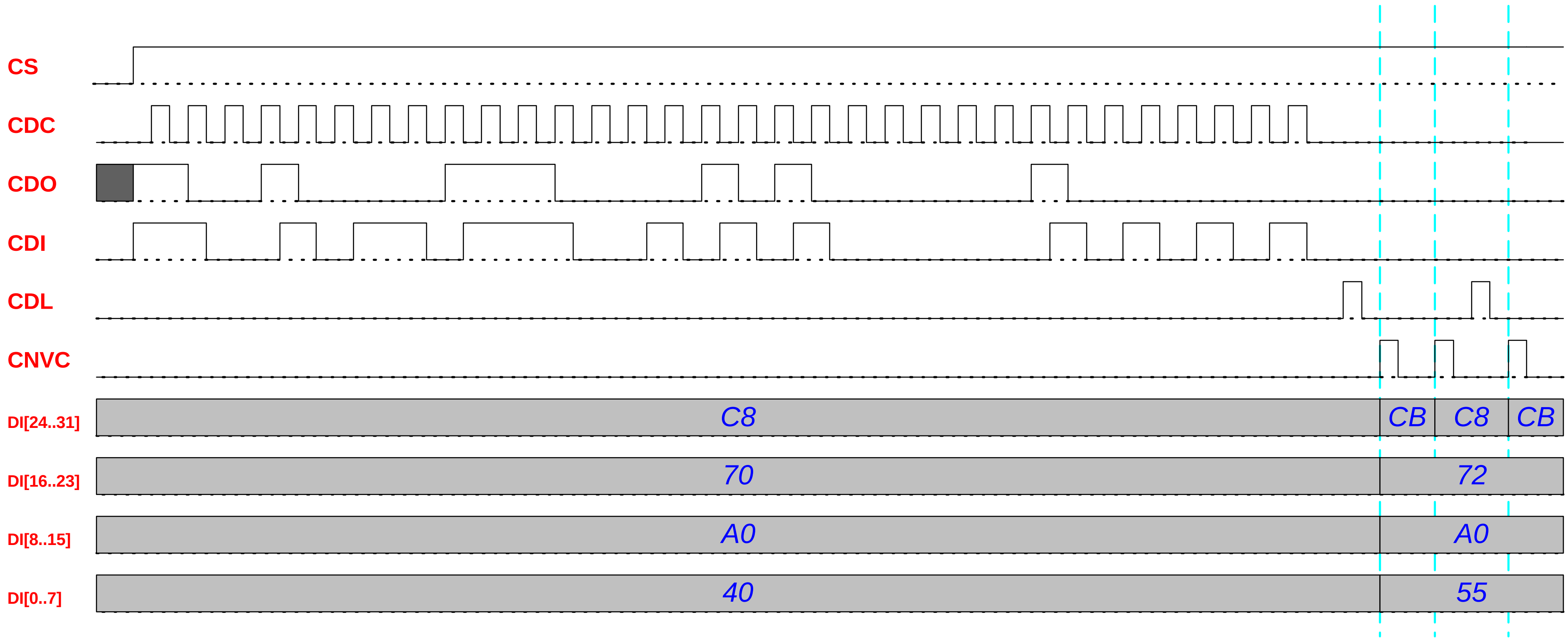


Figure 2

Sampled Data Output Timing Diagram

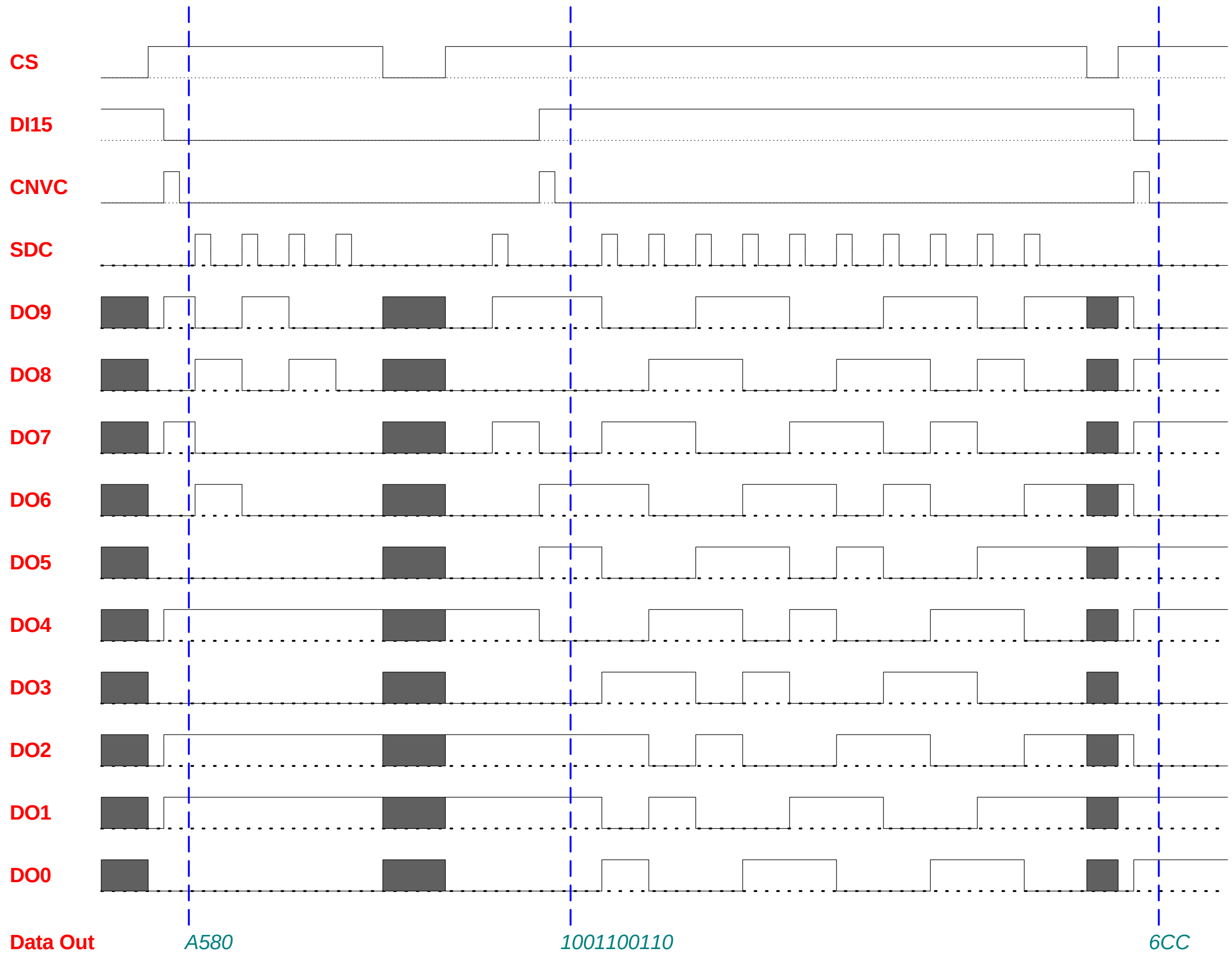


Figure 3